## AMENDMENTS TO THE SPECIFICATION

The following paragraphs will replace all prior versions of these paragraphs in the application:

#### <u>Abstract</u>

A method for inspecting electrical circuits, and a system for carrying out the method, generating a representation of boundaries of elements in an image of an electrical circuit which is under inspection, and analyzing at least some locations of at least some boundaries in the representation of boundaries of elements to identify defects in the electrical circuit.

## Paragraph 55 (paragraph at page 7)

[0055] Also in accordance with a preferred embodiment of the present invention, the providing step includes providing to the image processor parsed information relating to boundaries in the region of interest. Preferably, the providing step additionally includes providing providing a color image of the region of interest to the image processor.

#### Paragraph 113 (paragraph at page 12)

[0113] FIG. 50 is a simplified block diagram illustrating a a root process manager, constructed and operative in accordance with a preferred embodiment of the present invention;

### Paragraph 165 (paragraph at pages 17 and 18)

[0165] Scanner 2 is preferably an image illumination and acquisition system as described in Applicant's copending U.S. patent application Ser. No. \_\_\_\_\_09/565,500 entitled Illumination for Inspecting Surfaces of ObjectsArticles", and filed on May 5, 2000, now issued as U.S. patent No. 6,437,312. Although scanner 2 is preferably operative to acquire RGB optical images, it is readily appreciated that scanner may be operative to acquire other forms of image, for example monochrome gray level images, images in HIS

(Hue, Saturation and Intensity) format, or images correlating to non-optical properties of the object such as electric fields surrounding a printed circuit boards which define certain electrical properties relating to electrical circuits on the printed circuit board. It is appreciated that the present invention may relate to image processing of any suitable optical or non-optical image.

### Paragraph 174 (paragraph at page 20)

[0174] In accordance with a preferred embodiment of the present invention, a spatial area of interest identifier 6 is provided to define recurring spatial areas of interest in an inspected object. Spatial areas of interest are regions existing in object 4, in which a specific type of feature is expected to be present, and for which a predefined inspection routine tailored to the specific type of feature is typically performed.

# Paragraph 197 (paragraph at page 25)

[0197] Downstream of the HIP unit 38 is a SIP (Software Image Processing) unit 40 which receives the above 5 inputs from the HIP 38 unit and performs image processing operations as described in detail below. It is appreciated that while SIP is preferably implemented in software, it may be implemented in other at least partially programable programmable environments, such as DSPs and the like. The output of the SIP typically comprises a plurality of images and defect reports (corresponding to defect report 30 in FIG. 1A) which may be displayed to the user on the screen of his workstation 32.

# Paragraph 459 (paragraph at page 59)

[0459] width (15 bits) specifies the the width measurement of the width defect.

## Paragraph 530 (paragraph at page 66)

[0530] A line width reference comprises a set of rectangles, each of which encloses an area in an image within which all line width measurements have approximately of the same value. In areas where the widths of the lines have a high degree of change, it is typically not possible to create a suitable line width reference. The learn line width task

preferably is operative to identify the regions where a high level of change in line widths makes it impractical to form a line width reference. These areas are enclosed in rectangular areas which are identified as areas for which line widths ean can not be learned.

# Paragraph 663 (paragraph at page 81)

[0663] Step 1100: each CEL 1110 located in an inspection window 1120 is checked, and those CELs 1110 that are inside one or more envelopes 1130 surrounding reference ployline polyline 1240 are identified and appropriately tagged;